one sample is expressed with M bits ($M \neq N$);

converting the third digital information data generated in said encoding step, into fourth digital information data that plural samples are expressed with N bits; and

selectively adding an error correction check code to the second digital information data and the fourth digital information data,

said error correction step performing a common addition processing irrespectively of the second digital information data and the fourth digital information data. --.

REMARKS

Claims 31-33 and 35-37 are pending in the application. Claims 31, 32, 33 and 37 have been amended and claim 36 has been cancelled. Attached hereto is a marked-up version of the changes made to the claims by this Amendment. This marked-up version has been entitled "Attachment A – Marked-Up Version Showing Claim Amendments."

The Examiner has rejected applicant's claims 31-33 and 35-37 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. With respect to applicants' claims, as amended, this rejection is respectfully traversed.

Claims 31 and 37 have been amended to avoid this rejection. In particular, these claims now recite a digital information coding apparatus and corresponding method, respectively, including a step or unit for selectively inputting first digital information data and second digital

input data, one sample of each of which is expressed with N bits; an encoding step or encoder arranged to encode the first digital information data to generate third digital information data, one sample of which is expressed with M bits, a converting step or converter arranged to convert the third digital information data into fourth digital information data, plural samples of which are expressed with N bits; and an error correction step or unit arranged to selectively add an error correction check code to the second digital information data and the fourth digital information data and performing a common processing irrespective of such second and fourth digital information data.

Applicants' Specification clearly describes the features of the invention as now claimed in claims 31 and 37. Particularly, with reference to Figure 2 of the Application, the claimed input unit corresponds to the output lines of the A/D converters supplying 8-bit data (Application page 14, lines 19-23 and page 15, lines 22-26). The claimed encoder corresponds to compressor 14 as described in the Specification: "a sub-sampling circuit or a known high efficiency encoding circuit or the like is usable as the band compressor 14" for compressing the frequency band of a digital luminance signal output from 8-bit data to 4-bit data (Application page 15, lines 2-13). The claimed converter corresponds to converter buffer 16, described in the Specification as "memory circuit 16 which functions as a bit converter and a buffer," which converts plural 4-bit data into 8-bit data (Application Page 15, lines 13-20). Finally, the claimed error correction unit corresponds to ECC encoders 54-1, 54-2 and 54-3 to which data read out from the RAM is distributed as described in the Specification (Application page 19, line 3, through page 20, line 12).

As the Examiner well knows, the claims of the subject application are to be construed in light of the description in the specification as a whole and the specification need only provide "a reasonable amount of guidance with respect to how to practice a desired embodiment of the invention claimed." PPG Indus., Inc. v. Guardian Indus. Corp., 75 F.3d 1558, 1564 (Fed. Cir. 1996). Applicants, having demonstrated above the correspondence between the description in the applicants' specification and the elements in applicants' amended claims 31 and 37, thus submit that such claims, and their respective dependent claims, satisfy the requirements of 35 U.S.C. § 112, first paragraph.

The Examiner has also rejected applicants' claims 31-33 and 35-37 under 35 USC § 103(a) as unpatentable over Yoshimura et al. (U.S. Patent No. 5,012,352) in view of Official Notice. With respect to applicants' claims, as amended, this rejection is respectfully traversed.

As noted by the Examiner, the Yoshimura et al. patent discloses a digital signal recording apparatus having a coding apparatus for coding first data and second data and for recording the coded first and second data, including means for receiving the first and second data (video input terminal 10 and audio input terminals 16, 18), means for coding the first and second data (encoding circuits 14, 26), means for converting the first and second coded data (synchronization adding circuit 30) and error correcting means (ECC addition circuits 104, 108).

With respect to independent claims 31 and 37, the Examiner states that the error correction means taught by the Yoshimura et al. patent corrects video and audio signals. However, the Examiner acknowledges that the reference fails to specifically teach that the error correction means is used after converting the first data, but he states that shifting a part from one position to

another to perform the same function of error correcting the data would be obvious to one of ordinary skill in the art. With regard to the common error correction of first and second data, the Examiner concludes that "it would have been obvious to one of ordinary skill in the art to modify Yoshimura by using the error correction means and integrating the error correction means as an integral part to providing a common error correction means for error correcting the converted first parallel data and second parallel data."

Applicants submit that the Yoshimura et al. reference does not disclose or suggest the digital information coding apparatus and method as now claimed in the amended claims. More particularly, the Yoshimura et al. patent fails to specifically teach error correction of second and fourth digital information data as claimed. Particularly, the cited reference neither discloses nor suggests an encoder and converter or an encoding and converting step as claimed in the present invention, which makes it possible for the common error correction of second and fourth digital information data, the second and fourth data having the same number of bits representing a different number of samples, i.e. "second digital information data that one sample is expressed with N bits" and "fourth digital information data that plural samples are expressed with N bits." Further, the cited reference neither teaches nor suggests the claimed apparatus or method including processing digital information data with different numbers of bits representing one sample, i.e., encoding "first digital information data that one sample is expressed with N bits" to generate "third digital information data that one sample is expressed with M bits ($M \leq N$)," and converting the third digital information data into fourth digital information data as discussed above.

In summary, it is submitted that independent claims 31 and 37 are patentable based upon the Yoshimura et al. reference not disclosing or suggesting the content of the amended claims within the meaning of Section 103. Moreover, relying upon the patentability of the independent claims, the dependent claims 32, 33 and 35 are also submitted as being patentable since they differ in scope from the parent independent claims.

In view of the above, it is submitted that applicants' claims, as amended, patentably distinguish over the cited art of record. Accordingly, reconsideration of the claims is respectfully requested.

If the Examiner believes that an interview would expedite consideration of this Amendment, a request is made that the Examiner telephone applicants' counsel at (212) 682-9640.

Dated: October 22, 2002

Respectfully submitted,

John J. Torrente

Robin, Blecker & Daley
330 Madison Avenue
New York, NY 10017
(212) 682-9640

John J. Torrente
Reg. No. 26,359
Attorney for Applicant

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ATTACHMENT A - Marked-Up Version Showing Claim Amendments

In The Claims:

Amend claim 31 as follows:

-- 31. (Twice Amended) A digital information coding apparatus, comprising:

a) an input unit, arranged to selectively input [a first parallel data of N bits representing a] first digital information data that one sample is expressed with N bits and [second parallel data of N bits representing a] second digital information data that one sample is expressed with N bits[, wherein a bit rate of the first digital information differs from a bit rate of the second digital information];

b) an encoder, arranged to encode the first [parallel] digital information data to generate third [parallel] digital information data [of] that one sample is expressed with M bits [($M \neq N$)] ($M \leq N$);

c) a converter, arranged to convert the third [parallel] digital information data generated by said encoder, into fourth [parallel] digital information data that plural samples are expressed with [of] N bits; and

d) an error correction unit, arranged to selectively add an error correction check code to the second [parallel] digital information data and the fourth [parallel] digital information data,

said error correction unit performing a common addition processing irrespectively of second [parallel] digital information data and the fourth [parallel] digital information data. --.

Amend claim 32 as follows:

-- 32. (Amended) An apparatus according to claim 31, wherein said encoder encodes the first [parallel] digital information data to be encoded by differential pulse code modulation. --.

Amend claim 33 as follows:

-- 33. (Amended) An apparatus according to claim 31, wherein the second digital information data is a television signal in which a video signal and an audio signal are time-division multiplexed. --.

Cancel claim 36.

Amend claim 37 as follows:

-- 37. (Twice Amended) A digital information coding method, comprising:

selectively inputting [a first parallel data of N bits representing a] first digital information data that one sample is expressed with N bits and [second parallel data N bits representing a] second digital information data that one sample is expressed with N bits [, wherein a bit rate of the first digital information differs from a bit rate of the second digital information];

encoding the first [parallel] digital information data to generate third [parallel] digital information data [of] that one sample is expressed with M bits ($M \neq N$);

converting the third [parallel] digital information data generated in said encoding step, into fourth [parallel] digital information data [of] that plural samples are expressed with N bits; and

selectively adding [a predetermined data amount of] an error correction check code [for every predetermined data amount of] to the second [parallel] digital information data [or] and the fourth [parallel] digital information data,

said [adding] error correction step performing a common addition processing irrespectively of the second [parallel] digital information data and the fourth [parallel] digital information data. --.